400G OSFP AOC Specification

OSFP 400G to OSFP 400G AOC

Features

✧ **OSFP Serial Optical Interface**

- 4x100G PAM4 retimed 400GAUI-4 electrical interface
- Active Optical cable
- 4 channel VCSEL arrays and 4 channels PIN photo detector arrays
- Maximum link length of 60m on OM3 or 100m on OM4

✧ **OSFP MSA Compliant**

- Hot Pluggable OSFP form factor
- Compliant to OSFP Module Specification Rev 5.0
- Compliant with CMIS 5.2

✧ **Support Protocol**

- Compliant with IEEE 802.3db
- Compliant to IEEE 802.3ck

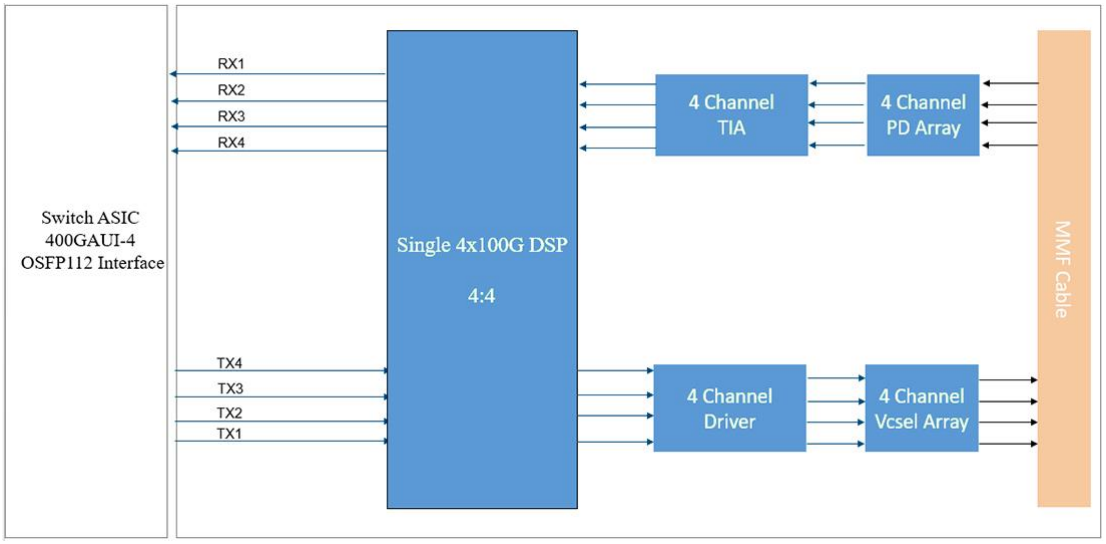
✧ **Low Power Consumption**

- Less than 8W in temperature range of 0 to 70℃

Applications

- 400GBASE-AOC 400G Ethernet
- Data center
- InfiniBand

Functional Block Diagram （each end）



1. General Description

The 400G AOC is a OSFP to OSFP active optical cable for short-range data communication and interconnect applications. Each AOC has 4 duplex channels with 425Gbit/s aggregate bandwidth. Each channel operates with PAM4 modulation scheme at 53.125G baud rate, and up to 60m using OM3 fiber or 100m using OM4 fiber

2. Absolute Maximum Ratings and Recommended Operating Conditions

（Table 2.1 Absolute Maximum Ratings）

Parameter	Symbol	Min	Max	Unit
Storage Temperature	Ts	-40	85	°C
Case Operating Temperature	Top	0	70	°C
Relative Humidity (non-condensation)	RH	15	85	%
Supply Voltage	Vcc	-0.5	3.6	V

（Table 2.2 Recommended Operating Conditions）

Parameter	Symbol	Min	Max	Unit
Operating Case Temperature	Top	0	70	°C
Relative Humidity(non-condensing)	RH	15	85	%

Power Supply Voltage	Vcc	3.135	3.465	V
Total Power Consumption	Pc	-	8	W
Supply Current per end			2.55	A
Bit Rate	BR		425	Gbps
I2C Clock Frequency	0		400	kHz

Notes:

1. Under condition of 3.465V operating supply voltage, and 70℃case temperature

3. Electrical Specification

(Table 4.1 Electrical Specifications)

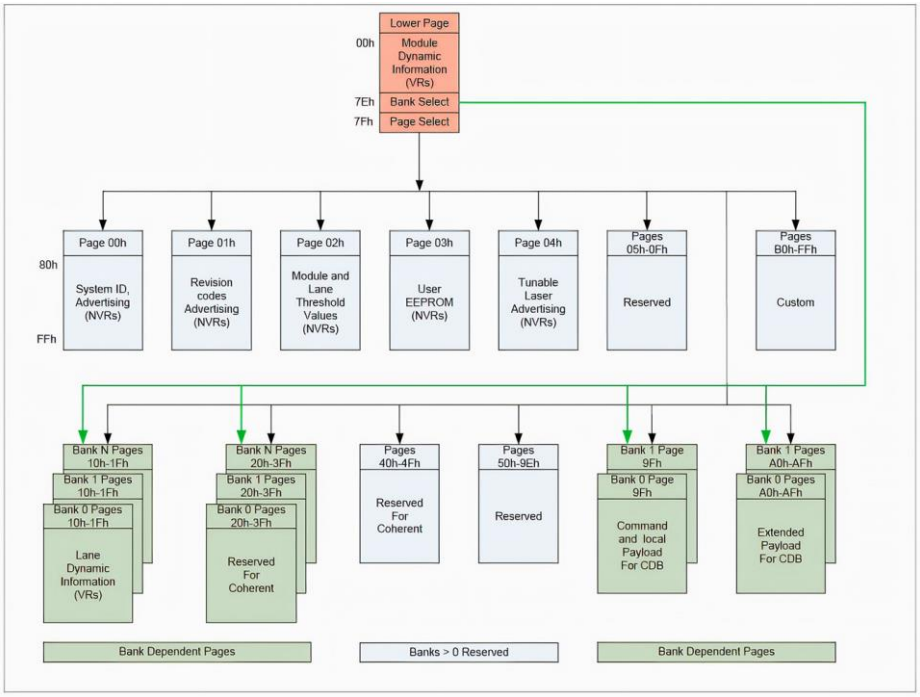
Parameter	Min	Typical	Max	Unit
Pre FEC Bit Error Ratio			2.4E-4	
Post FEC Bit Error Ratio			1E-12	
Transmitter (each Lane)				
Differential pk-pk Input Voltage tolerance	750			mV
Differential Termination Mismatch			10	%
Eye height	10			mV
Common-mode to differential-mode return loss	IEEE802.3ck Equation (120G–1)			dB
Vertical eye closure			12	dB
Effective return loss	7.3			dB
Transition Time	10			ps
Receiver (each Lane)				
Differential data output swing	300		900	mVpp
Differential termination mismatch			10	%
Eye height	15			mV
Vertical eye closure			12	dB
Common-mode to differential-mode return loss	IEEE802.3ck Equation (120G–1)			
Effective return loss	8.5			dB

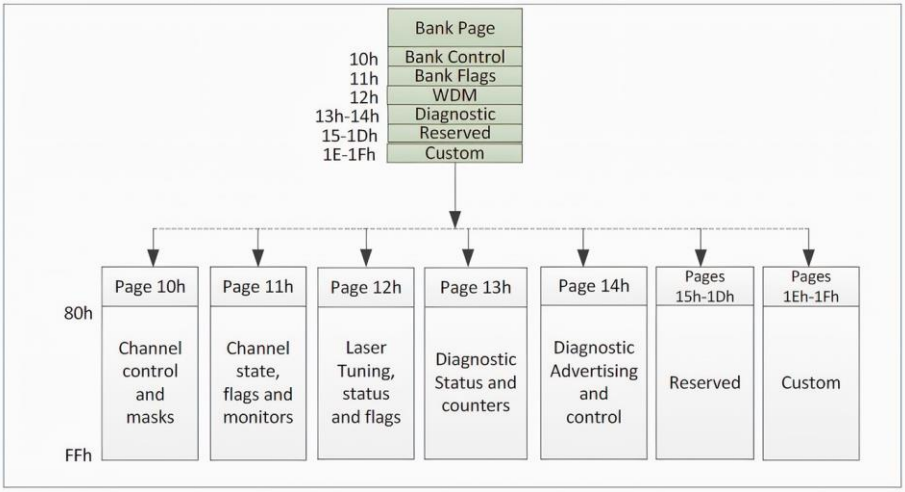
Transition time	8.5			ps

4. User Interface

4.1 Management Interface

2-Wire Serial Address: 1010000x（A0H）





(Figure 4.1 CMIS Module Memory Map)

4.2 Multiple Applications Support

The 400G AOC supports CMIS 5.2 defined Application Advertising, Application Selection and Instantiation.

4.2.1 Application Advertising

(Table 4.2 400G AOC Application Advertising)

Address (Dec)	Application		Value (Hex)	Description
	AppSel Code	Name		
85	NA	Module Type encoding	4	Optical Interfaces: AOC
86	0001b	HostInterfaceID	4B	HostInterfaceIDApp1:100GAUI-1-S C2M
87		MediaInterfaceID	3	MediaInterfaceIDApp1: BER 2.6E-4
88		HostLaneCount&MediaLaneCount	11	LaneCountApp1：TX & RX 1 lanes
89		HostLaneAssignmentOptions	F	Permissible first host lane number: lanes 1, 2, 3, 4
01h:176		MediaLaneAssignmentOptions	F	Permissible first media lane number: lanes 1, 2, 3, 4
90	0010b	HostInterfaceID	F	HostInterfaceIDApp2:200GAUI-4
91		MediaInterfaceID	2	MediaInterfaceIDApp2: BER 2.6E-4
92		HostLaneCount&MediaLaneCount	44	LaneCountApp2:TX & RX 4 lanes
93		HostLaneAssignmentOptions	1	Permissible first host lane number: lane 1
01h:177		MediaLaneAssignmentOptions	1	Permissible first media lane numbern: lane 1
94	0011b	HostInterfaceID	C	HostInterfaceIDApp3:100GAUI-4 C2M
95		MediaInterfaceID	2	MediaInterfaceIDApp3: BER 5E-5
96		HostLaneCount&MediaLaneCount	44	LaneCountApp3:TX & RX 4 lanes
97		HostLaneAssignmentOptions	1	Permissible first host lane number: lane 1
01h:178		MediaLaneAssignmentOptions	1	Permissible first media lane number: lane 1
98	0100b	HostInterfaceID	4F	HostInterfaceIDApp3:400GAUI-4 C2M
99		MediaInterfaceID	3	MediaInterfaceIDApp3: BER 2.6E-4
100		HostLaneCount&MediaLaneCount	44	LaneCountApp3:TX & RX 4 lanes
101		HostLaneAssignmentOptions	1	Permissible first host lane number: lane 1
01h:179		MediaLaneAssignmentOptions	1	Permissible first media lane number: lane 1
102	0101b	HostInterfaceID	4D	HostInterfaceIDApp4:200GAUI-2-S C2M
103		MediaInterfaceID	3	MediaInterfaceIDApp4:BER 2.6E-4
104		HostLaneCount&MediaLaneCount	22	LaneCountApp4:TX & RX 8 lanes
105		HostLaneAssignmentOptions	5	Permissible first host lane number: lane 1.3
01h:180		MediaLaneAssignmentOptions	5	Permissible first media lane number: lane 1.3
106		HostInterfaceID	FF	HostInterfaceIDApp5
107		MediaInterfaceID	0	MediaInterfaceIDApp5
108		HostLaneCount&MediaLaneCount	0	LaneCountApp5
109		HostLaneAssignmentOptions	0	Permissible first host lane number
110				

As shown in the table above，the 400G AOC supports 5 applications, 400GBASE-AOC, 200GBASE-AOC,100GBASE-AOC , 2x200GBASE-AOC and 4x100GBASE-AOC

4.2.2 Application Selection and Instantiation

The host can select Applications by programming the AppSel value in Staged Set 0. AppSel=1 is the default Application populated in the Active Control Set at power-on or reset.

*Note that the channels of the module are independent and can be configured separately. (ie. up to eight 100GBASE-SR instances can be configured), however, it does not support different applications with different channels at the same time

400G AOC supports two methods of application selection and instantiation. The first method is implemented according to CMIS, and the second method is customized，which is simpler.

■ **First mothod:**

The applications switching configuration sequence is as follows: read Application Descriptor Registers and select the required Appsel. Write application configuration to DPConfigLane<i> in Stage Control Set 0, then write 1 to ApplyDPInitLane<i> to trigger Application Instantiation. The Active Set can be read from page11h.

For example, select AppDescriptor3:

Step 1: Write 0x30 in Page10h Byte145~Byte152(8 bytes)—Set AppselCode3

Step 2: Write 0xFF in Page10h Byte143—Set trigger register to run Application Instantiation.

■ **Second mothod:**

Set the value of Page10h Byte240.This is a private definition.

(Table 4.3 Private Host Electrical Interface Codes)

Code Value	Bit Pattern	Host Electrical Interface	Media Interface
0	00000000b	100GAUI-1-S C2M	AOC
1	00000001b	200GAUI-4	AOC
2	00000010b	100GAUI-4	AOC
3	00000011b	400GAUI-4-S C2M	AOC
4	00000100b	200GAUI-2-S C2M	AOC

5.3 TX & RX Squelch

Default TX and RX auto-squelch is enabled. But TX and RX auto squelch disable, and force squelching function are not supported.

5.4 TX input equalization

Default TX adaptive equalization is enabled. But TX adaptive equalization disable, and fixed equalization adjust function are not supported.

5.5 RX output Equalization

RX output Equalization follows CMIS Table 6-7, with default 1dB, readable and writable

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000b	0dB (No Equalization)	0dB (No Equalization)
1	0001b	1 dB	0.5 dB
2	0010b	2 dB	1.0 dB
3	0011b	3 dB	1.5 dB
4	0100b	4 dB	2.0 dB
5	0101b	5 dB	2.5 dB
6	0110b	6 dB	3.0 dB
7	0111b	7 dB	3.5 dB
8-10	1000b-1010b	**Reserved**	**Reserved**
11-15	1011b-1111b	Custom	Custom

(Table4.5 OSFP Rx Output Equalization code table)

4.6 RX output amplitude

RX output amplitude follows CMIS Table 6-8, Rx output amplitude is the difference peak-to-peak EYE high when Rx output equalization is set to 0dB. The default value of output amplitude is set to 2, with typical differential 600mVp-p.

Code Value	Bit pattern	Output Amplitude
0	0000b	100-400 mV (P-P)
1	0001b	300-600 mV (P-P)
2	0010b	400-800 mV (P-P)
3	0011b	600-1200 mV (P-P)
4-14	0100b-1110b	**Reserved**
15	1111b	Custom

(Table4.6 OSFP Rx Output Amplitude code table)

4.7 Loopback capabilities

Media side input loopback and Host side input loopback feature are supported, loopback control method refers to CMIS.

(Table4.7 QSFP-DD Rx Output Equalization code table)

Byte	Bits	Field Name	Field Description
13h:128	6	Simultaneous Host And Media Side loopbacks	0b: not supported
	5	Per Lane Media Side Loopbacks	1b: supported
	4	Per Lane Host Side Loopbacks	1b: supported
	3	Host Side Input Loopback	1b: supported
	2	Host Side Output Loopback	1b: supported
	1	Media Side Input Loopback	1b: supported
	0	Media Side Output Loopback	1b: supported

4.8 Digital Diagnostic Monitor Accuracy

The following characteristics are defined over recommended operating conditions.

(Table 5.4Digital Diagnostic Monitor Accuracy)

Parameter	Parameter	Parameter
Internally measured transceiver temperature[1]	+/-3	°C
Internally measured transceiver supply voltage	+/-3	%
Measured Tx bias current	+/-10	%
Measured Tx output power[2]	+/-3	dB
Measured Rx received average optical power	+/-3	dB

Notes:

1. Test point is the hotspot of the module.

2. DDM reports stability within 0.5 dB when temperature is stable. TX DDM reportes -40 dBm when TX disable.

5. Pin Assignment and Description

5.1 PIN Definitions

OSFP Transceiver Pad Layout, host PCB OSFP Pinout, and PIN Descriptions are as follows:

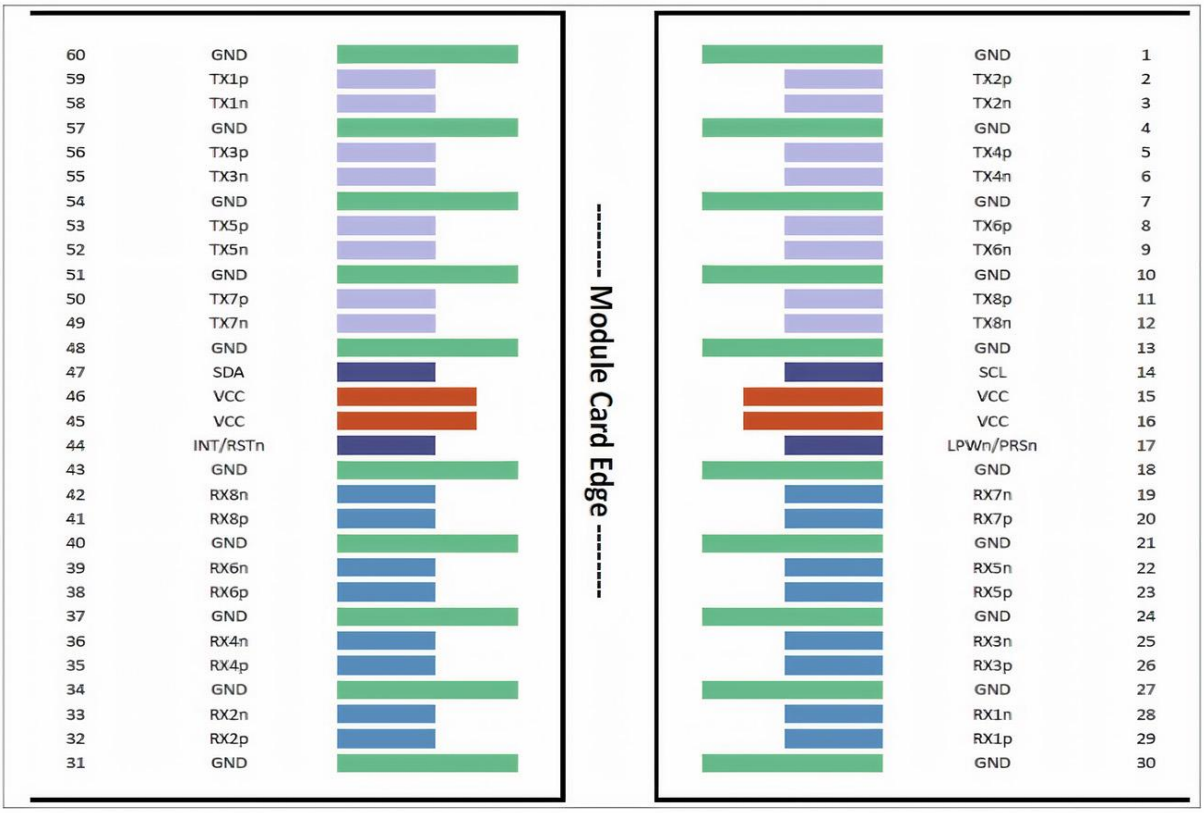


Figure 5.1 OSFP Transceiver Electrical Pad Layout

5.2 Pin Description

Table 5.2 Pin Description

Pin	Name	Logic	Description	Plug Sequence	Notes
1	GND		Ground	1	
2	Tx2p	CML-I	Receiver Data Non-Inverted	3	
3	Tx2n	CML-I	Receiver Data Inverted	3	
4	GND		Ground	1	
5	Tx4p	CML-I	Receiver Data Non-Inverted	3	
6	Tx4n	CML-I	Receiver Data Inverted	3	
7	GND		Ground	1	
8	Tx6p	CML-I	Receiver Data Non-Inverted	3	
9	Tx6n	CML-I	Receiver Data Inverted	3	
10	GND		Ground	1	
11	TX8p	CML-I	Receiver Data Non-Inverted	3	
12	TX8n	CML-I	Receiver Data Inverted	3	
13	GND		Ground	1	
14	SCL	LVCMOS-I/O	2-wire Serial interface clock	3	
15	VCC		+3.3V Power	2	
16	VCC		+3.3V Power	2	
17	LPWn/PRSn	Multi-Level	Low-Power Mode / Module Present	3	1A
18	GND		Ground	1	
19	RX7n	CML-O	Receiver Data Inverted	3	
20	RX7p	CML-O	Receiver Data Non-Inverted	3	
21	GND		Ground	1	
22	RX5n	CML-O	Receiver Data Inverted	3	
23	RX5p	CML-O	Receiver Data Non-Inverted	3	
24	GND		Ground	1	
25	RX3n	CML-O	Receiver Data Inverted	3	
26	RX3p	CML-O	Receiver Data Non-Inverted	3	
27	GND		Ground	1	
28	RX1n	CML-O	Receiver Data Inverted	3	
29	RX1p	CML-O	Receiver Data Non-Inverted	3	
30	GND		Ground	1	
31	GND		Ground	1	
32	RX2p	CML-O	Receiver Data Non-Inverted	3	
33	RX2n	CML-O	Receiver Data Inverted	3	
34	GND		Ground	1	
35	RX4p	CML-O	Receiver Data Non-Inverted	3	
36	RX4n	CML-O	Receiver Data Inverted	3	
37	GND		Ground	1	
38	RX6p	CML-O	Receiver Data Non-Inverted	3	
39	RX6n	CML-O	Receiver Data Inverted	3	
40	GND		Ground	1	

41	RX8p	CML-O	Receiver Data Non-Inverted	3	
42	RX8n	CML-O	Receiver Data Inverted	3	
43	GND		Ground	1	
44	INT/RSTn	Multi-Level	Module Interrupt / Module Reset	3	1B
45	VCC		+3.3V Power	2	
46	VCC		+3.3V Power	2	
47	SDA	LVCMOS-I/O	2-wire Serial interface data	1	
48	GND		Ground	3	
49	TX7n	CML-I	Transmitter Data Inverted	3	
50	TX7p	CML-I	Transmitter Data Non-Inverted	3	
51	GND		Ground	1	
52	TX5n	CML-I	Transmitter Data Inverted	3	
53	TX5p	CML-I	Transmitter Data Non-Inverted	3	
54	GND		Ground	1	
55	TX3n	CML-I	Transmitter Data Inverted	3	
56	TX3p	CML-I	Transmitter Data Non-Inverted	3	
57	GND		Ground	1	
58	TX1n	CML-I	Transmitter Data Inverted	3	
59	TX1p	CML-I	Transmitter Data Non-Inverted	3	
60	GND		Ground	1	

Notes:

1. Plug Sequence specifies the mating sequence of the host connector and module. The contact sequence is 1,2,3.
2. LPWn/PRSn is a Multi-level signal for low power control from host to module and module presence indication from module to host. It designed according to OSFP Module Specification Section 13.5.3
3. INT/RSTn is a Multi-level signal for interrupt request from module to host and reset control from host to module. It designed according to OSFP Module Specification Section 13.5.2

6. Mechanical Dimensions

6.1 Package dimensions

Figure 6.1 shows the package dimensions of the module. Package dimensions are specified in OSFP MSA.

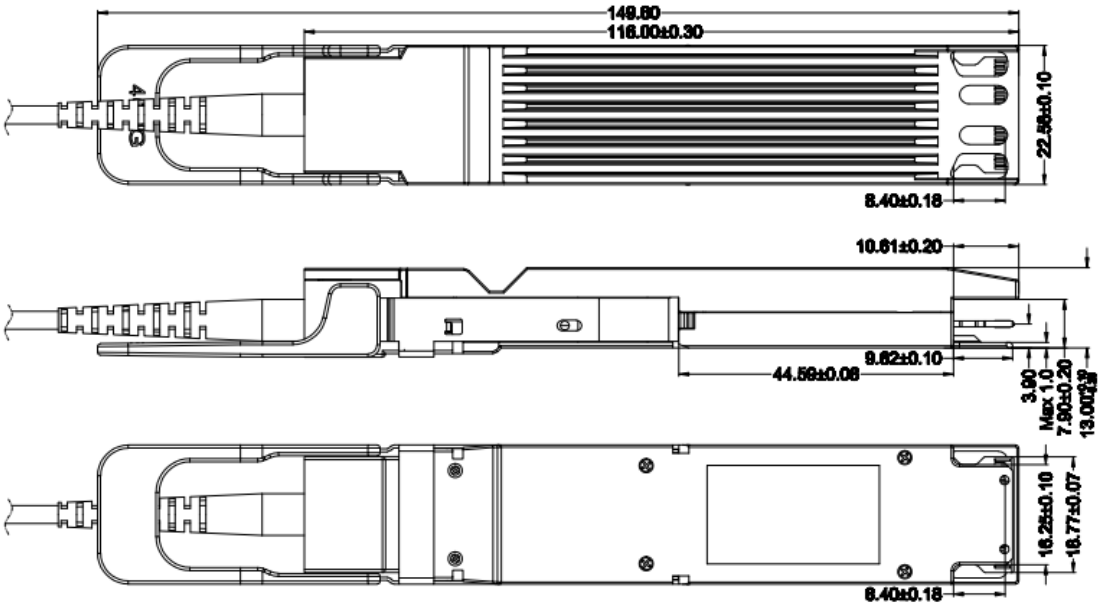


Figure 6.1 Package dimensions

6.2 Pull-tab Color

Pull-tab color is Pantone 475U (Beige).

Figure 6.2 Package dimensions

7. Laser safety and Electromagnetic Compatibility

7.1 Laser safety

The 400G AOC are Class 1 Laser products according to FDA/CDRH、IEC-60825-1 and IEC60825-2 standards. They must be operated under the specified operating conditions

7.2 Electromagnetic Compatibility

The 400G AOC C are designed to meet FCC Class B limits.

8. Ordering Information

Part Number	Temperature Range	Distance	Fiber Type	E/O	O/E
ROSFP-400G-AOC-1M	0 to 70℃	1m(OM3)	MMF	VCSEL 850nm	PIN
ROSFP-400G-AOC-3M	0 to 70℃	13m(OM3)	MMF	VCSEL 850nm	PIN
ROSFP-400G-AOC-10M	0 to 70℃	10m(OM3)	MMF	VCESL 850nm	PIN
ROSFP-400G-AOC-60M	0 to 70℃	60m(OM3)	MMF	VCESL 850nm	PIN